Journal of Expert Systems (JES)
Vol. 1, No. 2, 2012

www.worldsciencepublisher.org

2.4GHz Transceiver Design using ADS

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Abstract: The paper presents a transceiver design for 2.4GHz ISM band on HPADS (Hewlett Packard Advance Design System) using QAM modulation and pi/4DQPSK encoding scheme. The design software is presumed to be preferred for RF related applications. It has two different schemes DSP and Analog/RF design. These two schemes can be interfaced if required using co-simulation tool. Although the design proposed in this paper is made utilizing DSP scheme only. The paper takes a very conventional approach. First the design procedure has been explained, then parameters tuning and at last simulations results are presented and there by the paper would be concluded.

Keywords: ADS; EIRP; IF; RF; Data Flow Controller

1.Introduction

Transmitter and receiver stands as the most essential part in design of a system. The transmitter is where the data is going to be generated. Especially in case of the satellite it is the transmitter that gives the figure of merit of a system in terms of EIRP. The transmitter is supposed to cater for the issues as the power required at the other end, the gain that the antennas should have such that the signal reaches the destination with least amount of errors etc. The receiver is another crucial stage particularly in case of wireless transmission because the data that reaches the receiver is most likely to be erroneous due to numerous factors as atmospheric attenuation, polarization, diffraction, multipath effect etc. At the receiver end, the figure of merit is G/T_s which basically takes into account two important parameters, that is the receiver gain and the system temperature. With all the processing done at the receiver end, the next step is to look how much the data has been distorted once it has been retrieved at the final stage. The system qualification for this purpose is BER. The BER (Bit Error rate) takes two inputs normalize them and calculates the rate of mismatch between them. The QAM modulation scheme has been used with pi/4 DQPSK encoding. In the interim stages of both transmission and reception the filters have been used so that any data lost can be recovered to the receiver end. The Root Raised Cosine filters to fulfill the purpose of pulse shaping have been selected. Roll-off factor for the

filter is essential as this would depict the amount that our filter would deviate from its idealized response. Antenna has been used as the link designed is wireless. The controller required for the purpose of this simulation is Data Flow Controller. Any numeric start and stop along with start and stop time can be set in this block. The more the time would be set in this block the more the bits are going to be sent and the more it going to take long. With transmission and reception the one and foremost facility that the software offers is the real time data plots display. In this way the user can have a better understanding of how the process is taking place and where the changes have to be made, in case it is not in accordance to what is desired. ADS provide the facility of viewing different eye diagrams, constellation etc that adds to its unique feature's list. The design of this transmitter and receiver for 2.4 GHZ RF frequency came as a result of substantial amount of calculations. The IF frequency chosen for the design is 70MHz. Advantages associated with the modulation and encoding schemes are going to be discussed in the design procedure. At last the simulation results are going to be presented with which the user can have better understanding of the whole design.

2. Design Procedure

At first the data has to be generated for the purpose of transmission over the channel. The data source that we used is a random bit pattern with probability of 0.5 for both ones and zeros. The source can be selected under the *Numeric Sources* category. The bit pattern is then converted to non return-to-zero logic using logic to NRZ block. The block can be found under the *Signal Converters* category.
The data has been generated, the logic that it has -1 and 1. To avoid basing with subsequence DC residuals the data is then converted into a time based sequence using the block float to time. It can be found under the same *Numeric Sources* category. Basically we are going towards converting this digital signal into a continuous time signal so that later it can be transmitted through the antenna. The

next step is to interpolate the signal. The purpose of interpolation is to oversample the signal which can be done by making samples in-between the original baseband samples of the signal. The block can be found under *Timed Linear* category. The signal is then divided into two parts using data splitter. The block can be found under *Timed Data Processing* category. The signal now has two parts; each part is going to be encoded separately to avoid any interference to the data once it has been transmitted. The encoded scheme which we have selected is pi/4 DQPSK i.e. Differential Quaternary Phase Shift Keying. The advantage of using this scheme is that it is a Differential Encoding. Non coherent detection can easily be carried out at the other end since the scheme does not require the knowledge of the carrier phase while receiving. Using QPSK scheme was another option but the disadvantage it has is the maximum phase change that can occur from transmission to transmission is of π radians. This phase change can invert the signal and can lead to significant errors since the instantaneous amplitude fluctuation is very high. On the other hand $\pi/4$ DQPSK gives a maximum phase change of $3\pi/4$ rad. This leads to small instantaneous amplitude fluctuations. We know that the lesser these fluctuations are going to be, the lesser the regeneration of side lobes would be and lesser the signal would be distorted. Keeping in view these factors we selected $\pi/4$ DQPSK encoder present under *Timed Data Processing* category. Splitting and encoding would add some noise to the signal, the signal needs some pulse shaping now, the filters that fulfill this purpose are raised cosine LPF under the *Timed Filter Category*. The roll off factor for this filter is crucial as this would be the amount our filter would deviate from its idealized response.

The data has been encoded and filtered , now the time is to modulate it. Using QAM modulation the advantage that we have is that it can carry multiple signals over the same carrier. Since we are having two signals from the encoder, one *I-channel* and the other *Q-channel*, the scheme remains best suitable. Different choices of modulation schemes are available under *Timed Modem* category. The user can select the one that remains most appropriate for his design. All the processing from the IF section has been done and now is the time to shift this baseband signal into the pass-band so that it can be transmitted over the link. The block used for this purpose is RF-TX under *Timed RF Subsystems* category. The RF signal can now be transmitted either via an antenna or any waveguide depending upon whether the link is wireless or wired. If we consider the link to be wireless, antenna can be selected from *Antenna and Propagation* category other wise the medium can even be left wired. The antenna options that we have under this category are cellular mobile antenna, base station stationary antenna and array antenna. The antenna that we selected is base station stationary antenna with height of 10m. Users can select the gain and its other parameters depending upon their requirement. The transmitter portion has been completed and now is the time to receive it from the other end via channel or the medium.

The channel portion includes the antenna that has been discussed and with it there must be some noise associated as well. To keep the process simple we have selected default KT noise floor by choosing the block AddNDensity under *Timed RF Subsystem* category. The data that is coming is in pass-band, the first step would be to bring it to baseband for further processing. By selecting RF-IF block under *Timed data Subsystems* category we bring the data down to baseband. There by we demodulate it using QAM_Demod block under *Timed Modem* category. The data after modulation was single lined; the demodulator splits the data into the same two components *I-channel* and *Q-channel*. The received data has noise as well as the useful information. The first step would be to perform pulse shaping using raised cosine LPF present under *Timed Filter* category. The two *I* and *Q* channels are then inserted into pi/4 DQPSK decoder block under *Timed Data Processing* category. The block takes two inputs and decodes these two using the same scheme. All the processing from the receiver end has been performed and now is the time to convert the parallel data into serial form for the purpose of the BER calculation. This binary combiner can be found under *Timed Data Processing* category. Now it is the time to look for the errors in the signal received, for this purpose we consider a second path. Interpolation was the point from where we started all our processing so we take data after interpolation and compare it with that received. In addition to it we need to add some delay and gain that would compensate for all the processing i.e. modulation, encoding, decoding etc. The delay and gain blocks can be selected from *Timed Linear and Numeric Math* categories respectively The delay that we calculated was of 24 bit's time i.e. 493.8µs, adding this delay won't be enough so we need to add some gain to bring both the signals to the same 2,-2 logic. There by we compare the two signals using BER block present under *Sinks* category. For viewing plots in time and frequency domain at different points in the circuit the same *Sinks* palette can be visited.

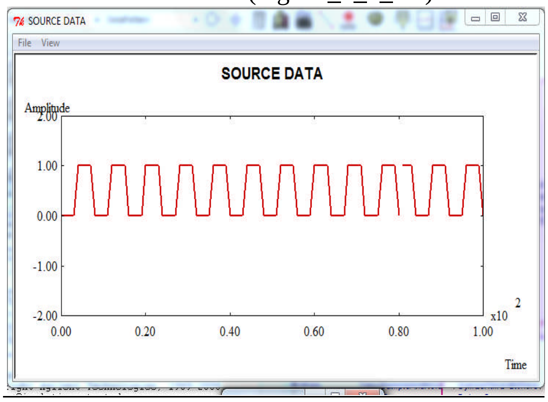
3.Setting up the Parameters

The RF frequency for the design proposed is 2.4GHz. Step time has been taken equal to the bit time for the float to timed block. The IF frequency or the carrier frequency is set to 70MHz, the carrier power is set 0.01W and the saturated power is set to 20W. The IF bandwidth for the system is set to 150KHz. Bit rate for the design is 48.6 KHz and the symbol time is 2*bit time, since in QPSK one symbol is represented by two bits. To fulfill the purpose of reducing ISI cancellation and maximizing SNR, RRC filters were used with pulse equalization and their corner frequency is set to (¼) of bit rate. The roll-off factor for all four filters (2 each for transmission and reception) is set to 0.35 and the window type is Hanning, which simply is a cosine based window. Transmitter gain is 80dB and receiver gain is set to 50dB. The receiver input power is kept equal to 3.2µW with noise figure being 5dB. Noise density in the system is set to default value of -174dbm/Hz. The delay and gain in the feedback path is set to 493.8µs and 1.5dB respectively. The controller for the circuit was

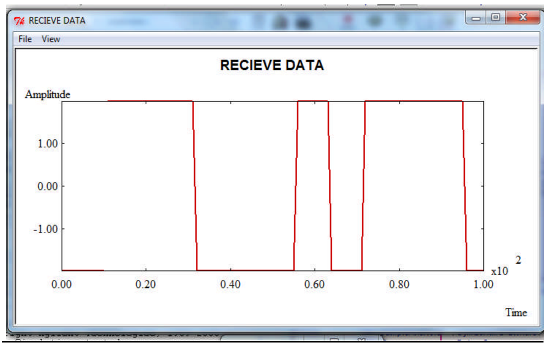
DF (data flow controller) under *Controllers* category which primarily gives the start and end time of simulation.
Once the simulation runs successfully the TK plot if attached from *Interactive Controls and Displays* category would occur showing data transmit and receive in real time as shown below. Note that logic 4_1_4_0 has been taken as input bit pattern only for this plot, just to make the data more understandable for the users, while for all the other plots the same random bit pattern of ones and zeros have been used. By choosing the New Data display option from the window drop down menu different the plots can be viewed

4.Simulation Results

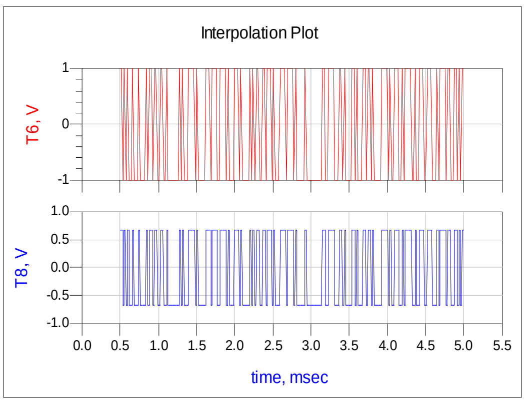
Source Data (logic 4_1_4_0...)



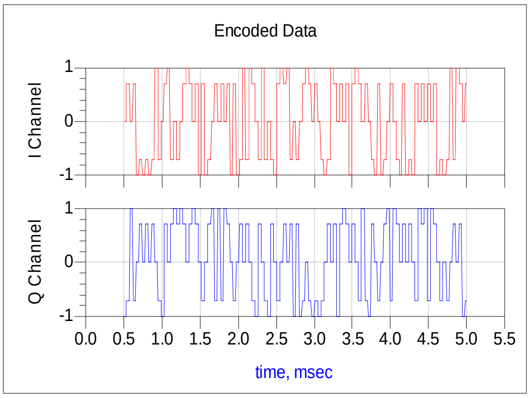
Receive Data



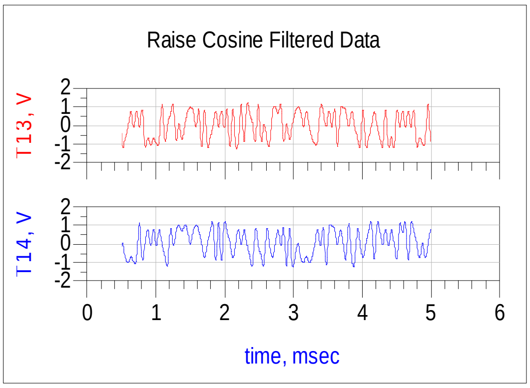
Interpolation Plot



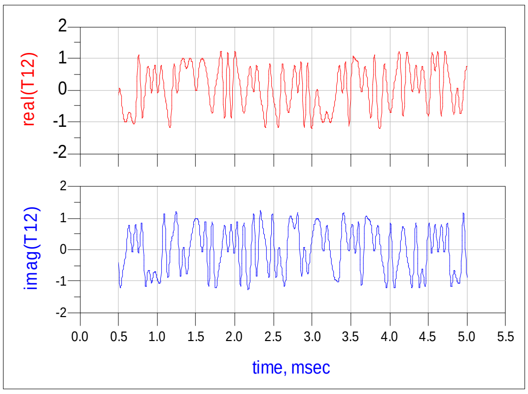
Encoded Data



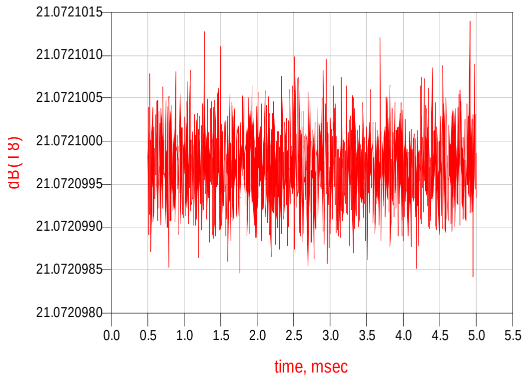
After RRC LPF



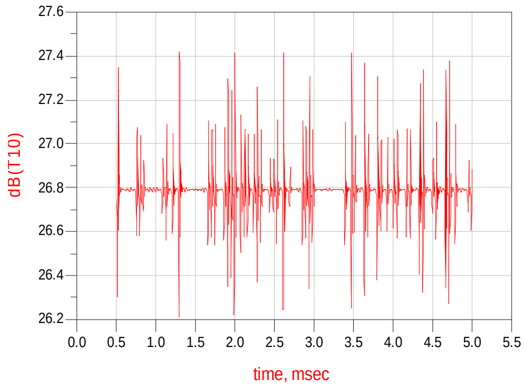
After Modulation



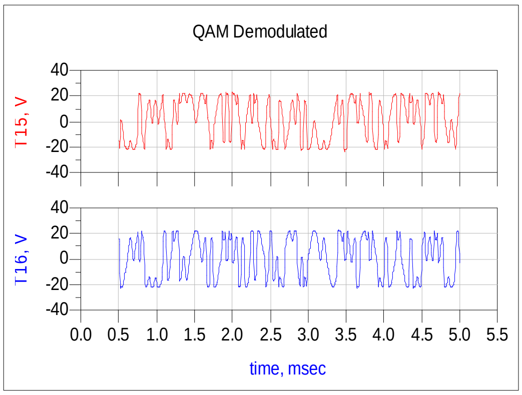
Transmitted Data



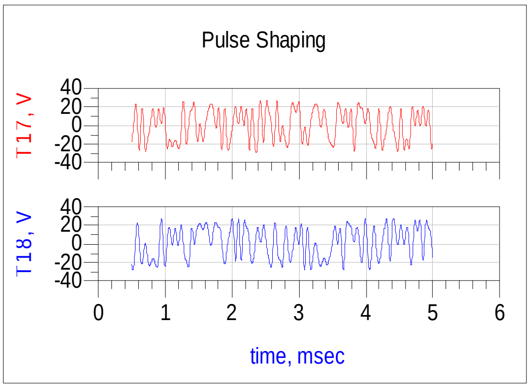
Received Data



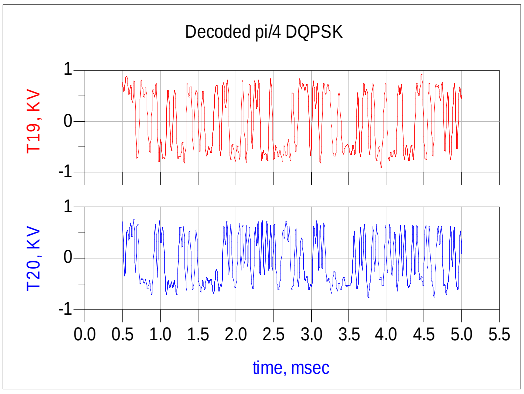
Demodulated Data



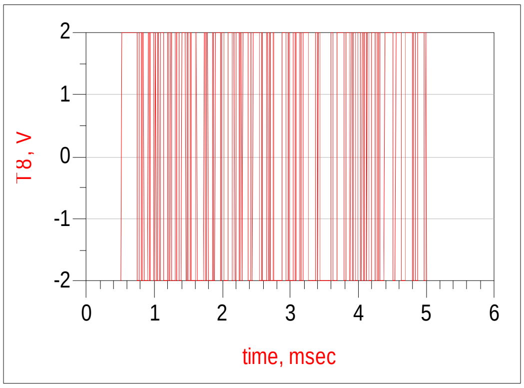
Pulse Shaping



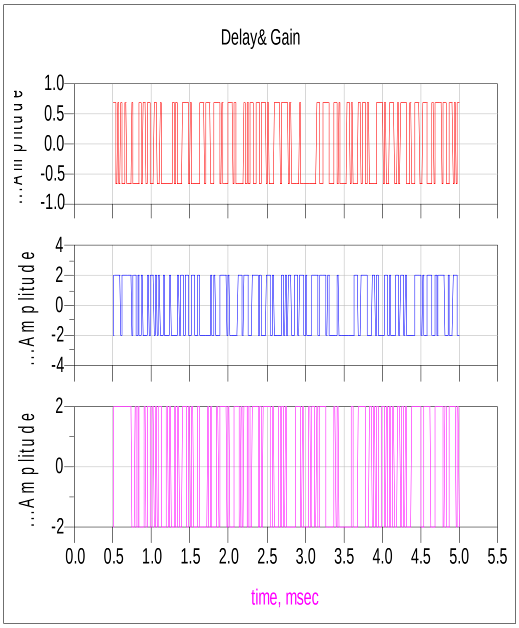
Decoded Data



After Binary Combiner



Delay and Gain



BER

Index	b1
0.000	0.247

5.Conclusion

The design has been anticipated as a guide for users particularly who are new to ADS. The BER received in the system is on the higher side but once the users get familiarized with the software they can make changes accordingly depending upon their requirements for the design and its application.

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